In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A multiply-accumulate module comprising:

a multiply-accumulate core, wherein said multiply-accumulate core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells, said plurality of Booth decoder cells including at least one first Booth decoder cell and at least one second Booth decoder cell, said at least one first Booth decoder cell structurally the same as said at least one second Booth decoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells, said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, said at least one first Wallace tree cell structurally the same as said at least one second Wallace tree cell;

wherein said multiply-accumulate module includes at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time;

wherein said at least one first Wallace tree cell or said at least one first Booth decoder cell are disposed on said at least one critical path;

wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are not disposed on any of said at least one critical path;

wherein said at least one first Wallace tree cell or said at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second Booth decoder cell comprises a second plurality of transistors; and

a width of at least one of said first plurality of transistors of said at least one first Wallace tree cell or said at least one first Booth decoder cell is greater than a width of a corresponding one of said second plurality of transistors of a corresponding one of said at least one second Wallace tree cell and said at least one second Booth decoder cell.

2. (Canceled)

3. (Previously Presented) The multiply-accumulate module of claim 1, wherein said multiply-accumulate core further comprises:

an adder connected to at least one of said Wallace tree cells;

a saturation detector connected to said adder, wherein said multiply-accumulate module further comprises:

at least one input register connected to at least one of said Booth encoding cells; and

at least one result register connected to said saturation detector.

4 to 8. (Canceled)

9. (Original) The multiply-accumulate module of claim 1, wherein said at least one second cell is a most significant bit or a least significant bit and said at least one first cell is not a most significant bit or a least significant bit.

10. (Previously Presented) A parallel multiplier comprising:

a parallel multiplier core, wherein said parallel multiplier core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells, said plurality of Booth decoder cells including at least one first Booth decoder cell and at least one second Booth decoder cell, said at least one first Booth decoder cell structurally the same as said at least one second Booth decoder cells; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells, said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, said at least one first Wallace tree cell structurally the same as said at least one second Wallace tree cell;

wherein said multiply-accumulate module includes at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time;

wherein said at least one first Wallace tree cell or said at least one first Booth decoder cell are disposed on said at least one critical path;

wherein said at least one second Wallace tree cell and said at least one second Booth decoder cell are not disposed on any of said at least one critical path;

wherein said at least one first Wallace tree cell or said at least one first Booth decoder cell comprises a first plurality of transistors, and at least one second Wallace tree cell or at least one second Booth decoder cell comprises a second plurality of transistors; and

a width of at least one of said first plurality of transistors of said at least one first Wallace tree cell or said at least one first Booth decoder cell is greater than a width of a corresponding one of said second plurality of transistors of a corresponding one of said at least one second Wallace tree cell and said at least one second Booth decoder cell.

11. (Canceled)

12. (Previously Presented) The parallel multiplier of claim 10, wherein said parallel multiplier core further comprises:

an adder connected to at least one of said Wallace tree cells;

a saturation detector connected to said adder, wherein said parallel multiplier further comprises:

at least one input register connected to at least one of said Booth encoding cells; and

at least one result register connected to said saturation detector and at least one of said Wallace tree cells.

13 to 17. (Canceled)

18. (Original) The multiply-accumulate module of claim 10, wherein at least one second cell is a most significant bit or a least significant bit and at least one first cell is not a most significant bit or a least significant bit.

19. (Previously Presented) A method of designing a multiply-accumulate module comprising the steps of:

providing a multiply-accumulate core, wherein the step of providing a multiply-accumulate core comprises the steps of:

providing a plurality of Booth encoder cells;

connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;

connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;

defining at least one critical path within said multiply-accumulate module, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than ~~a~~ said longest amount of time;

defining a Wallace tree cell disposed on said at least one critical path as a first Wallace tree cell;

defining a Wallace tree cell not disposed on any of said at least one critical path as second Wallace tree cell;

defining a Booth decoder cell disposed on said at least one critical path as a first Booth decoder cell;

defining a Booth decoder cell not disposed on any of said at least one critical path as second Booth decoder cell;

constructing each first Wallace tree cell and each first Booth decoder cell of a first plurality of transistors, each first Wallace tree cell structurally the same as each second Wallace tree cell, and constructing each second Wallace tree cell and each second Booth decoder cell of a second plurality of transistors, each first Booth decoder cell structurally the same as each second Booth decoder cell;

selecting a first width for at least one of said first plurality of transistors of at least one of said first Wallace tree cell or said first Booth decoder cell; and

selecting a second width for at least one of said second plurality of transistors of a second Wallace tree cell corresponding to said at least one of said first Wallace tree cell or of a second Booth decoder cell corresponding to said first Booth decoder cell which is less than said first width of a corresponding one of said first plurality of transistors.

20. (Previously Presented) A method of designing a parallel multiplier comprising the steps of:

providing a parallel multiplier core, wherein the step of providing a parallel multiplier core comprises the steps of:

providing a plurality of Booth encoder cells;

connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;

connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;

defining at least one critical path within said multiply-accumulate module, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-

accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than ~~a~~ said longest amount of time;

defining a Wallace tree cell disposed on said at least one critical path as a first Wallace tree cell;

defining a Wallace tree cell not disposed on any of said at least one critical path as second Wallace tree cell;

defining a Booth decoder cell disposed on said at least one critical path as a first Booth decoder cell;

defining a Booth decoder cell not disposed on any of said at least one critical path as second Booth decoder cell;

constructing each first Wallace tree cell and each first Booth decoder cell of a first plurality of transistors, each first Wallace tree cell structurally the same as each second Wallace tree cell, and constructing each second Wallace tree cell and each second Booth decoder cell of a second plurality of transistors, each first Booth decoder cell structurally the same as each second Booth decoder cell;

selecting a first width for at least one of said first plurality of transistors of at least one of said first Wallace tree cell or at least one of said first Booth decoder cell; and

selecting a second width for at least one of said second plurality of transistors of a second Wallace tree cell corresponding to said at least one of said first Wallace tree cell or of a second Booth decoder cell corresponding to said first Booth decoder cell which is less than said first width of a corresponding one of said first plurality of transistors.